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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		08/18/03	
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(Use as many sheets as necessary)	Art Unit	2825	
	Examiner Name	ROSSOSHEK, YELENA	

Examiner	Cite	NON PATENT LITERATURE DOCUMENTS  Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of	
nitials*	No.1	the item (book, magazine, journal, senal, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	1	*Representing circuits more efficiently in symbolic model checking." Burch, J.R.; Clarke, E.M.; Long, D.E. ACM/IEEE 28th Design Automation Conference, 1991. Publication Date: June 17-21, 1991. On page(s): 403 – 407.	
	2	"Efficient Model Chacking by Automated Ordaring of Transition Relation Pertitions." Danial Galet , Itan Baer. Proceedings of the 6th International Conference on Computer Aided Verification. Publication Date: June 21-23, 1994. On page;61: 298-310.	
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	4	*Bordar-Block Triangular Form and Conjunction Schedule in Image Computation.* In-Ho Moon , Gary D. Hachtal, Fablo Somanzi. Proceedings of the Third International Conference on Formal Methods in Computar-Method Design. Publication Date: November 01-03, 2000. On pages[27:78-0].	
	5	"Efficiant BDD algorithms for FSM synthesis and varification." R. K. Ranjan, A. Aziz, R. K. Brayton, B. F. Plessier, and C. Pixtey. International Workshop for Logic Synthesis, May 1995. Lake Tehoe, CA.	
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